Listing of the Claims:

1. (Original) A clock generation circuit for an integrated circuit device comprising:

a temperature sensor circuit including a calibration circuit responsive to a temperature coding signal and a temperature sensor, the temperature sensor circuit having a first state in which a temperature output signal of the temperature sensor circuit is based on a temperature sensor output control signal and a second state in which the temperature output signal is based on the temperature sensor and the calibration circuit;

a clock period controller circuit, including a calibration circuit responsive to a period coding signal, that generates a period control signal based on the temperature output signal and the calibration circuit of the clock period controller circuit; and

a clock generator circuit that generates a clock signal based on the period control signal.

2. (Original) The circuit of Claim 1 wherein the calibration circuit of the temperature sensor circuit comprises a plurality of fuses and wherein the temperature coding signal selects a state of ones of the plurality of fuses to calibrate the temperature output signal relative to an output of the temperature sensor.

3. (Original) The circuit of Claim 2 wherein the calibration circuit of the clock period controller circuit comprises a plurality of fuses and wherein the period coding signal selects a state of ones of the plurality of fuses to calibrate the period control signal.

4. (Original) The circuit of Claim 2 wherein the first state or the second state of the temperature sensor circuit is selected based on the temperature sensor output control signal.

5. (Original) The circuit of Claim 4 wherein the temperature output signal comprises a digital signal having a plurality of states, ones of which correspond to temperature operating ranges of the integrated circuit device.

6. (Original) The circuit of Claim 5 wherein the first state comprises a test mode and the second state comprises a normal operating mode and wherein the temperature sensor output control signal comprises a plurality of bits that designate ones of the temperature operating ranges in the test mode.

7. (Original) The circuit of Claim 4 wherein the temperature sensor outputs a digital temperature signal based on a detected temperature of the integrated circuit device and wherein the temperature sensor circuit further comprises a multiplexer that outputs the temperature output signal based on the digital temperature signal from the temperature sensor and the temperature coding signal.

8. (Original) The circuit of Claim 7 wherein the digital temperature signal from the temperature sensor and the temperature sensor output control signal each comprise a plurality of bits, ones of which correspond to temperature operating ranges of the integrated circuit device.

9. (Original) The circuit of Claim 4 wherein the clock period controller circuit comprises a plurality of period controllers calibrated by the calibration circuit of the clock period controller circuit based on the period coding signal, at least one of the plurality of period controllers being selected by the temperature output signal to generate the period control signal.

10. (Original) The circuit of Claim 4 wherein the clock generator circuit comprises an oscillator that generates the clock signal with a period based on the period control signal.

11. (Original) The circuit of Claim 4 wherein the integrated circuit device comprises a memory device and wherein the clock signal comprises a refresh clock.

12. (Original) An integrated circuit memory device comprising:

a temperature sensor circuit including a calibration circuit responsive to a temperature coding signal and a temperature sensor that generates an operating temperature signal responsive to a temperature of the memory device and the calibration circuit, the temperature sensor circuit having a first state in which a temperature output signal of the temperature sensor circuit is based on a temperature sensor output control signal and a second state in which the temperature output signal is the operating temperature signal, the first state or the second state being selected by the temperature sensor output control signal;

a clock period controller circuit, including a calibration circuit responsive to a period coding signal, that generates a period control signal based on the temperature output signal and the calibration circuit of the clock period controller circuit; and

a clock generator circuit that generates a refresh clock of the memory device based on the period control signal.

13. (Original) The memory device of Claim 12 wherein the operating temperature signal and the temperature sensor output control signal each comprise a plurality of bits, ones of which correspond to temperature operating ranges of the memory device.

14. (Original) The memory device of Claim 12 wherein the clock period controller circuit comprises a plurality of period controllers calibrated by the calibration circuit of the clock period controller circuit based on the period coding signal, one of the plurality of period controllers being selected by the temperature output signal to generate the period control signal.

15. (Original) The memory device of Claim 12 wherein the clock generator circuit comprises an oscillator that generates the refresh clock with a period based on the period control signal.

16. (Original) A method for controlling the refresh period of an integrated circuit memory device comprising:

calibrating a temperature sensor circuit of the memory device to generate an operating temperature signal corresponding to an operating temperature of the memory device by inputting to the temperature sensor circuit a selected temperature coding signal;

selecting a test mode of the temperature sensor circuit in which a temperature output signal of the temperature sensor circuit is based on a temperature sensor output control signal or to select a normal operating mode of the temperature sensor circuit in which the temperature output signal is the operating temperature signal, the test mode or the normal operating mode being selected by the temperature sensor output control signal;

calibrating a clock period controller circuit of the memory device to generate a period control signal having a desired period by inputting to the clock period controller circuit a period coding signal, the period control signal further being based on the temperature output signal; and

generating a refresh clock of the memory device, the period of the refresh clock being based on the period control signal.

17. (Canceled).

18. (Currently Amended) ~~The~~ A semiconductor memory device ~~as claimed in claim 17,~~ comprising:

a temperature sensor including a plurality of fuses, the temperature sensor for receiving a sensor coding signal, thereby cutting the plurality of fuses, and generating an operational temperature signal, which indicates the real temperature at which the

semiconductor memory device operates, in response to a temperature sensor output control signal;

a clock period controller having a plurality of fuses, the clock period controller for receiving a period coding signal, thereby cutting the plurality of fuses, and generating a period control signal in response to the operational temperature signal;

a clock generator for receiving the period control signal and generating a refresh clock, the period of which is controlled in accordance to the operational temperature of the semiconductor memory device; and

wherein the temperature sensor output control signal comprises a plurality of bits, indicates whether the semiconductor memory device is in a test mode or a normal operating mode, and indicates the temperature range at which the semiconductor memory device operates.

19. (Currently Amended) ~~The~~ A semiconductor memory device ~~as claimed in claim 17,~~ comprising:

a temperature sensor including a plurality of fuses, the temperature sensor for receiving a sensor coding signal, thereby cutting the plurality of fuses, and generating an operational temperature signal, which indicates the real temperature at which the semiconductor memory device operates, in response to a temperature sensor output control signal;

a clock period controller having a plurality of fuses, the clock period controller for receiving a period coding signal, thereby cutting the plurality of fuses, and generating a period control signal in response to the operational temperature signal;

a clock generator for receiving the period control signal and generating a refresh clock, the period of which is controlled in accordance to the operational temperature of the semiconductor memory device; and

wherein the temperature sensor comprises:

a temperature sensor for outputting a sensor output signal including a plurality of bits by receiving the sensor coding signal and sensing the real operational temperature of the semiconductor memory device; and

a multiplexer for receiving the sensor output signal and generating the operational temperature signal according to logic values of the plurality of bits of the sensor output signal in response to the temperature sensor output signal.

20. (Original) The semiconductor memory device as claimed in claim 19, wherein the sensor coding signal comprises a plurality of bits and changes the sensing temperature of the temperature sensor.

21. (Original) The semiconductor memory device as claimed in claim 19, wherein the number of bits of the sensor output signal is the same as the number of bits of the temperature sensor output control signal.

22. (Currently Amended) ~~The~~ A semiconductor memory device ~~as claimed in claim 17,~~ comprising:

a temperature sensor including a plurality of fuses, the temperature sensor for receiving a sensor coding signal, thereby cutting the plurality of fuses, and generating an operational temperature signal, which indicates the real temperature at which the semiconductor memory device operates, in response to a temperature sensor output control signal;

a clock period controller having a plurality of fuses, the clock period controller for receiving a period coding signal, thereby cutting the plurality of fuses, and generating a period control signal in response to the operational temperature signal;

a clock generator for receiving the period control signal and generating a refresh clock, the period of which is controlled in accordance to the operational temperature of the semiconductor memory device; and

wherein the clock period controller is enabled by the operational temperature signal and comprises a plurality of period controllers that generate the period control signal by receiving the period coding signal.

23. (Original) The semiconductor memory device as claimed in claim 22 wherein the period coding signal comprises a plurality of bits and changes the period control signal generated from the clock period controller.

24. (Currently Amended) The semiconductor memory device as claimed in claim ~~17~~ 18, wherein the clock generator comprises an oscillator that generates the refresh clock, the period of which is controlled by the period control signal.

25. (Currently Amended) The semiconductor memory device as claimed in claim ~~17~~ 18, wherein the clock generator further comprises a counter that changes the period of the refresh clock by receiving an output signal of the oscillator.

26. (Canceled).

27. (Currently Amended) ~~The method as claimed in claim 26,~~ A method of controlling the period of a refresh clock in accordance to variations in the operational temperature of the semiconductor memory device that includes a temperature sensor having a plurality of fuses and a clock period controller, the method comprising the steps of:

(a) receiving a sensor coding signal, thereby cutting a plurality of fuses of the temperature sensor, and generating an operational temperature signal indicating the real temperature at which the semiconductor memory device operates;

(b) receiving a period coding signal, thereby cutting a plurality of fuses of the clock period controller, and generating a period control signal in response to the operational temperature signal; and

(c) receiving the period control signal and generating the refresh clock, the period of which is controlled in accordance to the operational temperature of the semiconductor memory device; and

wherein the temperature sensor output control signal comprises a plurality of bits and indicates the temperature range at which the semiconductor memory device operates and whether the semiconductor memory device is in a test mode or a normal operating mode.

28. (Currently Amended) ~~The method as claimed in claim 26,~~ A method of controlling the period of a refresh clock in accordance to variations in the operational temperature of the semiconductor memory device that includes a temperature sensor having a plurality of fuses and a clock period controller, the method comprising the steps of:

(a) receiving a sensor coding signal, thereby cutting a plurality of fuses of the temperature sensor, and generating an operational temperature signal indicating the real temperature at which the semiconductor memory device operates;

(b) receiving a period coding signal, thereby cutting a plurality of fuses of the clock period controller, and generating a period control signal in response to the operational temperature signal; and

wherein step (a) comprises the steps of:

(a1) outputting a sensor output signal including a plurality of bits by receiving the sensor coding signal and sensing the real operational temperature; and

(a2) generating the operational temperature signal according to logic values of a plurality of bits of the sensor output signal by receiving the sensor output signal and sensing the temperature sensor output control signal.

29. (Original) The method as claimed in claim 28, wherein the sensor coding signal comprises a plurality of bits and changes the temperature sensing temperature.

30. (Original) The method as claimed in claim 28, wherein the number of bits of the sensor output signal is the same as the number of bits of the temperature sensor output control signal.

31. (Currently Amended) The method as claimed in claim ~~26~~ 27, wherein step (b) comprises the steps of:

(b1) enabling one bit of the operational temperature signal; and

(b2) generating a period control signal by receiving the period coding signal, which controls the period of the refresh clock, in response to the enabled operational temperature signal.

32. (Original) The method as claimed in claim 31, wherein the period coding signal comprises a plurality of bits and changes the period control signal generated from the clock period controller.